

CLAIMS

1. An apparatus comprising:

an input circuit configured to generate a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

5 a storage circuit configured to store each of said data paths in a respective shift register chain; and

an output circuit configured to generate an output data signal in response to each of said shift register chains, wherein said output data signal presents said data items in a second order
10 different from said first order.

2. The apparatus according to claim 1, wherein said first order comprises a sequential presentation of said plurality of data items.

3. The apparatus according to claim 1, wherein said second order comprises a sequential presentation of said plurality of data items.

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4. The apparatus according to claim 1, wherein said input circuit comprises a demultiplexer circuit.

5. The apparatus according to claim 1, wherein said output circuit comprises a multiplexer circuit.

6. The apparatus according to claim 1, wherein said input circuit is controlled by a finite state machine.

7. The apparatus according to claim 1, wherein said output circuit is controlled by said finite state machine.

8. The apparatus according to claim 1, wherein each of said data paths is configured to have a propagation delay.

9. An apparatus comprising:

means for generating a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

5 means for storing each of said data paths in a respective shift register chain; and

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means for generating an output data signal in response to each of said shift register chains, wherein said output data signal presents said data items in a second order different from said first order.

10. A method for re-ordering data comprising the steps of:

(A) generating a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

(B) storing each of said data paths in a respective shift register chain; and

(C) generating an output data signal in response to each of said shift register chains, wherein said output data signal presents said data items in a second order different from said first order.

11. The method according to claim 10, wherein said first order comprises a sequential presentation of said plurality of data items.

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12. The method according to claim 10, wherein said second order comprises a sequential presentation of said plurality of data items.

13. The method according to claim 10, wherein step (A) generates said data paths using a finite state machine.

14. The method according to claim 13, wherein step (C) generates said output data signal using said finite state machine.

15. The apparatus according to claim 1, wherein each of said data paths is configured to have a propagation delay.

16. An apparatus comprising:

an input circuit configured to generate a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

5 a storage circuit configured to store each of said data paths in a memory; and

an output circuit configured to generate an output data signal in response to said memory, wherein said output data signal

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presents said data items in a second order different from said

10 first order.